

B.TECH 8th SEMESTER
ADVANCE PROCESS DYNAMICS AND CONTROL.
(EIE-402-E)

L T P
 4 1 -

Theory : 100
 Sessional : 50
 Time : 3Hrs

Unit I

ANALYSIS AND DESIGN OF ADVANCED CONTROL SYSTEMS: Review and limitation of single loop control, need of multi loops, cascade, selective override, auctioneering, split range, feed forward, feed forward feedback, adaptive, inferential, ratio control, Self adaptive control: MRAC, STR, dead time compensator.

Unit II

MULTI VARIABLE CONTROL: Interacting, non-interacting, stability, relative gain array method

STATE SPACE ANALYSIS: state variable, state space representation, observability, controllability, transfer function, relationship between observability, controllability and transfer function.

Unit III

COMPUTER BASED CONTROL SYSTEM: Introduction. Digital computer simulation of control system, computer control system, direct digital, supervisory, distributed digital control, microprocessor based control system.

PLC AND INSTRUMENTATION SYMBOL: Introduction to plc, relative merits over band wired logic and relays, programming language, PI diagram, standard instrumentation symbols, signal types.

Unit IV

ANALYSIS OF COMPLEX PROCESSES: Control of jacketed kettle systems, dynamic response of gas absorber, heat conduction into solids, heat exchanger.

NOTE:

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

References:

- i) Process System Analysis And Control By **Donald R. Coughanouer**
- ii) Introduction To Programmable Logic Controller By **Gary Duming**
- iii) Process Control Instrumentation Technology By **Curtis Johnson**
- iv) Process Control By **Bela G. Liptac**.

**B.TECH 8th SEMESTER
COMPUTER HARDWARE
(EIE-404-E)**

L T P
4 1 -

Theory : 100
Sessional : 50
Time : 3Hrs

UNIT I

MICROCOMPUTER SYSTEM:- Introduction, computer organization, Memory, Arithmetic & logic unit, Control unit, instruction prefetch, Interrupt, Input/output techniques, device controllers, error detection techniques, microprocessor, personal computer concepts & techniques.

PERIPHERAL DEVICES: - Introduction keyboard, CRT display monitor, printers, magnetic storage devices, floppy disk drive, hard disk drive, special peripherals

Unit II

PC Hardware Overview:- Introduction, hardware-BIOS-DOS Interaction ,the PC Family, PC Hardware, Interconnections between Boxes, Inside the system Box, Motherboard logic, memory space, I/O port address, peripheral interfaces & controllers, keyboard interface Parallel interface, serial interface, CRT display controller, floppy disc controller(FDC), Hard disc controller(HDC), hard disc card.

Unit III

MICROPROCESSORS IN PC:-Introduction, Intel 8088, Internal organization, bus cycle, 8088 operation, I/O addressing, Interrupt Handling, 8088 Instructions, co-processor.

Support chips in the Motherboard: Introduction, Dumb & smart chips, clock Generator 8284, bus controller 8259A, programmable interval timer 8253, 8255A-5 programmable peripheral interface(PPI), DMA controller 8237A-5.

Unit IV

MOTHERBOARD CIRCUITS:-Introduction, Motherboard Functions, functional units & Intercommunication reset logic, CPU nucleus logic, DMA logic, wait state logic, bus arbitration logic, RAM logic,ROM logic, ROM decode logic, RAM parity logic, NMI Logic I/O ports decode logic, time of delay (TOD) logic, dynamic memory refresh logic, speaker logic, mode switch input logic, Keyboard interface, co-processor unit, control bus logic, address bus logic, data bus logic, I/O slot signals, new generation motherboard, motherboard connectors and jumpers, SMPS

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BOOKS :

IBM PC & Clones – Hardware, Troubleshooting & MaintenanceBy:-B. GovindRajalu
Tata Mcgrah Hill Publishing Co. Ltd. New Delhi

B.TECH 8th SEMESTER
DATA COMMUNICATION AND COMPUTER NETWORK
(EIE-406-E)

L T P
4 1 -

Theory : 100
 Sessional : 50
 Time : 3Hrs

Unit I

Basic Concepts: Networking goals and applications , structure , architecture, ISO-OSI reference model , topology , example networks.

Physical Layer: The theoretical basis for data communication , Analog and digital transmission, ISDN , transmission media, transmission and switching.

Unit II

The Medium Access Sublayer: Aloha protocols, LAN protocols, IEEE standards, fiber optic networks, satellite

Networks , packet radio networks.

Data Link Layer: Design issues, error detection & correction; elementary data link protocols, Sliding window protocols, protocol performance.

Unit III

Network Layer: Design issues, routing algorithms, congestion control algorithms, internetworking

Transport and Session Layer: Protocol design issues, connection management, remote procedure calls.

Unit IV

Presentation Layer: Design issues, abstract syntax notation, data compression technique, Cryptograph.

Application Layer: Design issues, file transfer , access and management , electronic mail , virtual terminals , applications and examples.

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The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Books :

1. Tanenbaum A.S. : Computer Networks, PHI, 1990
2. Davics D.W.Barber: Computer Networks and their Protocols, John Wiley.
3. Bee K.C.S : Local Area Networks, NCC Publication.
4. Ahuja V : Design and Analysis of Computer Communication Networks, McGraw Hill.

B.TECH 8th SEMESTER
DEPARTMENTAL ELECTIVES-I
ENVIRONMENT MONITORING INSTRUMENTATION
(EIE-408-E)

L T P
 3 2 -

Theory : 100
 Sessional : 50
 Time : 3Hrs

UNIT-I

Air and water Pollution : Sources & Effects

Definition and concentrations, classification, emission sources, Air pollution standards, sources of pollutions, effects of Air pollution, Sources of contamination of surface and ground water.

UNIT-II

Air Pollution Sampling and Measurements

Ambient air sampling, Collection of gaseous air pollutants, Collection of particulate pollutants, stack sampling, Analysis of Air pollutants.

UNIT-III

Air Pollution Monitoring Instruments

Photometry, Mass spectrometry, NMR, X-ray Fluorescence, Infra red spectrometry, Flame photometry, Atomic absorption spectroscopy, chromatography, Coulometry etc. for measurement of SO₂, Nitrogen oxides, carbon monoxide, hydrocarbons and particulate matter.

UNIT-IV

Water Pollution sampling and Measurements and Monitoring Instruments

Sampling and Analysis , Samplers-Batters, Heavy metal and trace metal analysers, pH meters, Resistivity meters, Induced Polarisation(IP) Meter for monitoring of industrial contamination. waste water management and recycling equipments.

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Books recommended :

1. Environmental Pollution Control Engg. C S Rao ; New Age International.
2. Industrial Pollution. V P Kudesu; Pragati Prakashan.
3. Instrumental Methods of Analysis. Willaied, Meritt & Dean ; C B S Publishers.
4. Environmental Pollution Analysis. S M Khopkar ; New Age International.
5. Ground Water Hydrology David Keith Todd, Wiley Publications
6. Fundamentals of geophysics William Lowrie, Cambridge University press

**B.TECH 8th SEMESTER
DEPARTMENTAL ELECTIVES-I
REMOTE SENSING
(EIE-410-E)**

L T P
3 2 -

Theory : 100
Sessional : 50
Time : 3Hrs

Unit I:

Introduction, concept & foundations of remote sensing, Ideal remote sensing system, Methodology, Resolutions- spatial, Spectral Radiometric & Temporal, Spectral Signatures, Radiometric terms, stoke's parameter.

Unit II

Interaction of Electromagnetic Radiation with earth's surface & earth atmosphere. Air Photo interpretation- fundamentals & basic equipment. Aerial sensor Imagery, Multispectral scanners, Thermal IR line scanner, Sideway looking Airborne Radar (SLAR), Satellite sensor Imagery.

Unit III

Remote sensing related instrumentation & systems, IR spectrometer Radiometers, Scanners, LIDAR Detectors and systems, Photo Conductive, Photo diodes, CCD, PMT, Vidicon, Orthicon characteristics of detectors

Unit IV

Remote sensing applications- Oceanography, Mineral Resources, Forestry land use planning, weather Forecasting.

NOTE:

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Books :

1. Remote sensing & Image Interpretation by Lillesand, Kiefer : John wiley & sons, Inc.
2. Principles of Remote sensing (Paul J. Curran- ELBS/ Longman) P.N. Slater Addison- wesley.

**B.TECH 8th SEMESTER
DEPARTMENTAL ELECTIVES-I
FUZZY LOGIC AND APPLICATIONS
(EIE-412-E)**

L T P
3 2 -

Theory : 100
Sessional : 50
Time : 3Hrs

Unit 1: Introduction :

Fuzzy control from an industrial perspective, knowledge – based controller, knowledge representation in KBC's.

Unit 2: The Mathematics of fuzzy control: -

Vagueness, fuzzy logic versus probability theory, fuzzy sets, their properties and operation on fuzzy sets, fuzzy relation & operations on fuzzy relations, the extension principles, fuzzy propositions, the compositional rules of inference, different implications, representing a set of rules.

Unit 3: PKBC design parameters: -

The PKBC architecture, choice of variables and contents of rules, derivation of rules, choice of membership functions, choice of scaling factors, choice of fuzzification procedure, choice of defuzzification procedure, comparison and evaluation of defuzzification methods.

Unit 4: Adaptive fuzzy control: -

Design and performance evaluation, approaches to design such as membership function tuning using gradient descent, membership function tuning using performance criteria, the self organizing controller, model based controller.

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Books for Reference :

1. Fuzzy control system by Abraham Kandel and Gideon Imngholz; Narosa.
2. Fuzzy control system by D.Drainkov and M.Reienfrank.

B.TECH 8TH SEMESTER
DEPARTMENTAL ELECTIVES-II
MICROPROCESSOR AND INTERFACING (8086)
(EIE-414-E)

L T P
 3 2 -

Theory : 100
 Sessional : 50
 Time : 3Hrs

UNIT-I:

INTRODUCTION: Evolution of microprocessors, technological trends in microprocessor development. The intel family tree, CISC applications of Microprocessors.

8086 CPU ARCHITECTURE : 8086 block diagram: description of data registers, address registers; pointer and index registers PSW, queue BIU and EU, 8086 pin diagram descriptions generating 8086 CLK and reset signals using 8284 WAIT state generation. Microprocessor BUS types, 8086 minimum mode and maximum mode CPU module.

UNIT-II

8086 INSTRUCTION SET:- Instruction formats, addressing modes, data transfer instructions, string instructions, assembler directive, Writing assembly language programs

UNIT-III

MAIN MEMORY SYSTEM DESIGN:- Memory devices, 8086 CPU read/write timing diagrams in minimum mode and maximum mode. Address decoding techniques interfacing SRAMS, ROMS/PROMS. Interfacing and refreshing DRAMS DRAM controller-TMS4500.

UNIT-IV

BASIC I/O INTERFACE: Parallel and serial I/O port design and address decoding. Memory mapped isolated I/O, intel 8255 and 8251 description and interfacing with 8086, ADC and DAC types operation and interfacing with 8086. interfacing keyboard, alphanumeric displays, multiplexed display and high power devices with 8086.

Interrupts and DMA: interrupt driven I/O 8086 interrupt mechanism, interrupt types and interrupt vector table, intel 8259. DMA operation.

NOTE :

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

REFERENCES:

1. Hall DV, Microprocessor and Interfacing, IInd Edition, McGraw Hill.
2. Uffenbeck J, The 8086/8088 family, PHI
3. Liu Gibson, Microcomputer System – The 8086/8088 family, IInd Ed, PHI.

**B.TECH 8th SEMESTER
DEPARTMENTAL ELECTIVES-II
ADVANCED VLSI
(EIE-416-E)**

L T P
3 2 -

Theory : 100
Sessional : 50
Time : 3Hrs

Unit 1 :-

Introduction to MOS Technology: The integrated circuit era, CMOS fabrication: P-well process, n-well process, twin-tub process, BiCMOS fabrication, difference between CMOS technology and Bipolar technology.

Unit 2 :-

Basic electrical properties of CMOS and Bi CMOS circuit: CMOS inverter, BiCMOS inverter, latch up in CMOS circuits, BiCMOS latch up susceptibility, difference between parameters of CMOS and Bipolar transistor, CMOS inverter delay, driving large capacitive loads, BiCMOS drivers.

Unit 3:

CMOS and Bi CMOS circuit design processes: Stick diagram, CMOS design style, CMOS lambda based design rules, 2 micro meter (μm) double metal ,double poly CMOS/BiCMOS rules, 1.2 μm double metal, single poly CMOS rules.

Unit 4:

Subsystem design and layout: Two input CMOS and BiCMOS NAND and NOR gate, dynamic CMOS logic, clocked CMOS logic, CMOS domino logic, parity generator, bus arbitration logic for n- line bus, multiplexer, grey to binary code converter, dynamic shift register.

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The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Reference books:-

Basic VLSI design “Douglas.A.Pucknell” (prentice hall of India).
“Kamran Eshraghian” .

B.TECH 8th SEMESTER
DEPARTMENTAL ELECTIVES-II
VHDL
(EIE-418-E)

L T P
 3 2 -

Theory : 100
 Sessional : 50
 Time : 3Hrs

UNIT I

Intorduction: why use VHDL? Hardware design consatructrion, design levels, HDLs, hardware simulation and synthesis.using VHDL for design synthesis, terminology.

Programmable Logic devices: why use programmable logic? What is a programmable logic device? Block diagram, macro cell structures and characxterstics of PLDs and CPLDs. Architecture and features of FPGAs. Feature direction programmable logics.

UNIT II

BEHAVIOURAL modeling: entity, declaration, architecture body, process statement, variable assignment , signal assignment. Wait, if , case, NULL, LOOP,EXIT, NEXT and assertion statements. Inertiasl and transport delays, simulkation deltas, signal drivers.

DATA FLOW AND STRUCTURAL MODELING: Concurrent signal assignment, sequential signal assignment, multiple drivers, conditional signal assignment, selected signal assignment, block statement, concurrent assertion statement, component declaration, component instantiation.

UNIT III

GENERICs AND CONFIGURATION: Generic, Why Configuration? Default configuration, component configuration, Generic in configuration, Generic value specification in architecture, block configurations, architecture configurations.

SUBPROGRAMS AND PACKAGES: Subprograms- functions, procedures, declaration, package declaration, package body, use clause, predefined package standard, design libraries, design file.

UNIT IV

ADVANCED TOPICS: Generate statement, Aliases, Qualified expressions, Type conversion, Guarded signal, User defined attributes, Predefined attributes, VHDL synthesis.

NOTE:

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References:

- 1 Perry D, VHDL, 3rd Ed.- TMH.
- 2 Bhaskar J, A VHDL Primer, PHI
- 3 Skahil, VHDL for Programmable logic, 2nd Ed.-Wiley Publication.

**B.TECH 8th SEMESTER
COMPUTER HARDWARE LAB
(EIE-426-E)**

L T P
- 3

Exam : 25
Sessional : 50
Time : 3Hrs

LIST OF EXPERIMENTS

- 1 To solder and desolder various components.
- 2 To check and measure various supply voltages of PC.
- 3 To make comparative study of motherboards: 386,486,PI, PII, PIII
- 4 To observe and study various cables, connections and parts used in computer communication.
- 5 To study various cards used in system viz. display card, LAN card etc.
- 6 To remove, study and replace FDD.
- 7 To remove, study and replace HDD.
- 8 To remove, study and replace CD ROM drive.
- 9 To study monitor, its circuitry and various presets and some elementary fault detection
- 10 To study parts of keyboard and mouse.
- 11 To assemble a PC.
- 12 Troubleshooting exercises related to various components of computer like monitor, drives, memory, and printers etc.

NOTE: At least 11 experiments are to be performed with atleast 8 from above list, remaining 3 may either be performed from the above list or designed & set by concerned institution as per the scope of syllabus.