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Total No. of Questions : 8]

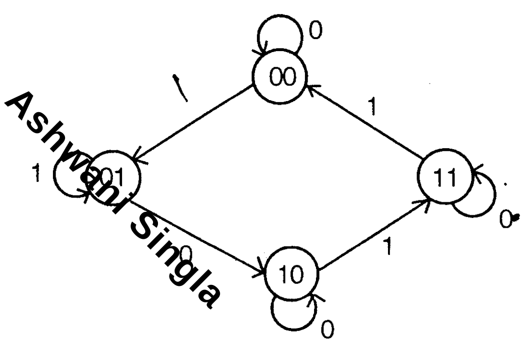
[Total No. of Printed Pages : 3

ECE–502
ELECTRONIC SYSTEM DESIGN
(M.Tech., 1st Semester, 2123)

Time : 3 Hours   Maximum Marks : 100

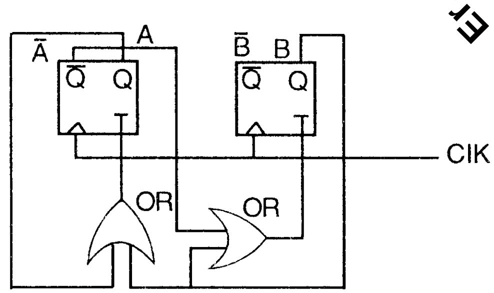
Note :– Attempt any *Five* questions.
All questions carry equal marks.

1. Write down the truth table for full subtractor circuit and realize it using :
   (a) NAND gates only
   (b) 4 : 1 multiplexer.
2. For the state diagram shown below, obtain the table and design the circuit using minimum number of J-K FFS.



3. (a) Design a sequence detector which produces an output 1 everytime the sequence 1011 is detected and an output 0 at all other times.

(b) Derive the state table and draw state diagram of the sequential circuit shown below. Mention the function of this circuit.



4. Design a synchronous counter using J-K flip-flops to count in the following sequence :

0, 2, 6, 10, 14, 2, 6, 10, ...

Your counter should avoid lockout condition.

5. (a) Define a finite state machine. What are its capabilities and limitations ?

(b) Design C hazard free combinational network to using NAND gates (Fan-in = 3) to implement the following min term :

$$f = \Sigma\, 2, 5, 6, 7, 10, 13, 15.$$

6. (a) What are the steps involved in a digital system design ? Explain them briefly.

(b) Design a PLA circuit to implement the following min term :

$$f = \Sigma\, 2, 5, 6, 7, 10, 13, 15.$$

7. (a) What is the necessity grounding and shielding of digital circuits ? Explain.

(b) Synthesize the function

$$f = \overline{A}\,\overline{B}C + A\overline{B}\,\overline{C} + A\overline{B}C + AB\overline{C} + ABC$$

using 16L8PAL.

8. Write short notes on the following :

(a) MSI Decoder

(b) Bus oriented structures

(c) MDS Diagram. 7,7,6