

ITEC-294, Digital Electronics

Time : 3 hrs.]

[Maximum Marks :75

Note : Attempt any five questions.

1. a) Express the following boolean equation in maxterm list form :

$$F(P, Q, R, S) = (P + Q)R' + P'S'R' + PQ'(S' + R' + Q') \quad 6$$

- b) Use Q-M procedure to minimize :-

$$F(A, B, C, D) = \sum m(0, 2, 4, 5, 6, 9, 10) + \sum d(7, 11, 12, 13, 14, 15) \quad 9$$

2. Design a detailed IC level circuit to display the data on eight BCD input lines on eight 7-segment displays (one for each digit). Assume that the data arrive on input lines 1 through 8 in eight consecutive time slots of $10 \mu s$ each. The data input cycle of $80 \mu s$ repeats with new data each cycle. 15

Draw TTL Buffer circuit. Also mention

- a) its input and output logic levels. 6
 b) Design MOD to UP/DOWN counter. 9

4. a) You are given JK flip-flop. Design the circuitry around it to convert it into i) T-flip flop, 6
 ii) D flip-flop, iii) S-R flip flop. 6

b) Draw a circuit diagram for the synchronous sequential circuit described by the following equations :

Output $Z = XY_1Y_2$

Flip-flop input $J_1 = XY_2, K_1 = X'$

$J_2 = X, K_2 = X' + Y_1$

5. Draw 8 bit serial 2's Complementor circuit. 9

a) Use state diagram approach. 6

b) For the following incompletely specified state tables, drive i) implication chart ii) maximal compatibles iii) maximal incompatibles and (iv) Reduced state table :

X_1, X_2

	00	01	11	10
A	A/0	B/-	A/0	C/-
B	B/0	D/1	C/-	A/-
C	C/0	E/1	C/0	E/-
D	D/0	E/0	E/-	-/-
E	E/0	-/-	C/1	E/-

9

6. a) Write the steps to design fundamental mode asynchronous circuits. 5

b) The internal asynchronous circuit of T-flip flop is to be designed. T and clock (c) are two inputs. Z is output if T is 1 and C changes from 1 to 0, the flip flop complements its output. In all other conditions, the output of the flip-flop remains unchanged. 10

7. a) Explain working of dual slope. ADC. Draw and explain sample and hold circuit. 7

b) Design 4 bit bipolar (signed) R-2R ladder type DAC. 8

8. Write short notes on the following :

a) Variable entered maps

b) CMOS logic.

8.7


