

Marks

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Roll No.

Total No. of Pages : 2

BT-4 / J04

8674

ITEC-264 : Digital Electronics

Time : 3 Hrs.

M.M. : 100

Note : (1) Attempt any five questions.

(2) All questions carry equal marks.

- I (a) Minimise F_1 and F_2 using VEM. 10
 $F_1 (A, B, C, D) = \Sigma (2, 4, 5, 10, 11, 13)$
 $d = \Sigma (0, 1, 6, 15)$
 $F_2 (A, B, C, D) = \Sigma (2, 3, 5, 6, 7, 14)$
 $d = \Sigma (10, 13)$
(b) Minimise $F = \Sigma (0, 3, 6, 7, 9, 11, 13, 15)$ using k-map.
Implement using NAND-gates only. 10
- II (a) Design a BCD to 7-segment code converter. 10
(b) Design a four bit parity checker/generator, that is, a circuit that can be used to check parity over a five word as well as generate the parity bit over a four bit word. 10
- III (a) Design a 5×32 decoder using four 3×8 decoders and one 2×4 decoder. 10
(b) Implement $F(A, B, C, D) = \Sigma (0, 2, 6, 8, 11, 13, 14, 15)$ using 8×1 mux. 10
- IV (a) Convert JK flip-flop to D and D to T flip-flop. 10

- (b) Design a JK flip-flop. Explain Race-around condition. **10**
- V Design an up-down counter using minimum no. of J-K flip-flops. **20**
- VI (a) Explain in detail the functioning of TTL-logic family.
 (b) Compare TTL, CMOS and ECL in terms of : **14,6**
 (i) Maximum fan-outs
 (ii) Lowest propagation delay
 (iii) Lowest power dissipation
- VII (a) Draw a block diagram of a ladder type D/A converter and briefly explain its operation. **10**
 (b) In a 10 bit D/A converter, the full scale o/p is +10v. Determine the output voltage for an input of **10**
 (i) all 1s
 (ii) only MSB = 1 and
 (iii) only LSB = 1
- VIII Write short notes on : **20**
 (a) Encoder
 (b) A/D converter
 (c) Shift Register
 (d) C-MOS